ejections to the Claims: 35 U.S.C. § 102(e)

The Examiner rejects claims 1-8 under 35 U.S.C. § 102(e) as being anticipated by Linke et al. (U.S. Patent No. 5,960,188) or Matsunaga (U.S. Patent No. 5,909,374). Applicant respectfully traverses these rejections for the reasons presented below.

The Invention

The present invention relates to a circuit simulation method and apparatus for simulating and inspecting a large-scale integrated ("LSI") circuit such as a MOS LSI circuit to satisfy design specifications and improve performance of the circuit. Because a MOS LSI circuit is large in scale, the circuit needs to be simplified while ensuring accuracy of circuit operation. Simplifying the circuit reduces the time required for simulation and enables high-speed simulation.

In one embodiment of the present invention, first, partial circuits are extracted from the circuit to be simulated. The partial circuits are inspected for equivalence. If the configurations of the partial circuits are consistent with each other, then the operational characteristics of the corresponding circuit elements are compared with each other. Next, if all pairs of corresponding circuit elements have the same operational characteristics, then the input and output terminals are compared with each other. If the corresponding input and output terminals are identical, then the operational characteristics of the partial circuits are considered to be equivalent. However, if the input or output terminals are not identical, then the partial circuits connected to the input or output terminals are inspected for quasi-equivalence. If the input or output terminals are quasi-equivalent circuits, the partial circuits are considered to be equivalent.

To distinguish partial circuits, the intensity of the influence of an external terminal of the extracted partial circuits upon the extracted partial circuits is taken into account. The intensity of the influence of the external terminal is assessed as the frequency of shifting from the source or drain of a MOS semiconductor device to the gate thereof in the course of tracing

a path linking the external terminals and an object terminal. Even if the connected states of corresponding external terminals of two partial circuits are mutually inconsistent, as long as the intensities of currents flowing from the external terminals placed in the inconsistent connected states are equal to or larger than a designated value, the influence of the external terminals is considered to be negligible. Consequently, the partial circuits are judged to exhibit equivalent operational characteristics.

After the circuit is compressed by integrating the partial circuits exhibiting the equivalent operational characteristics into one circuit, circuit simulation is carried out.

In conventional circuit simulation methods, only circuit elements located in a limited area within a circuit can be inspected to determine if they exhibit the same characteristics. It is difficult to distinguish all circuit elements exhibiting equivalent operational characteristics in the circuit. Thus, the circuit is not compressed effectively. In contrast, in the present invention, integrating a plurality of partial circuits into one circuit can be readily achieved. As a result, a circuit to be simulated can be compressed more effectively, reducing the scale of the circuit.

The References

Linke et al. Linke relates to a method and apparatus for verifying the correct performance of software on an electrical system using a cycle-based simulator. Linke simulates an electrical interconnection between two electronic subsystems, or modules, within a cycle-based simulator (Abstract). The simulator models, for example, a microcomputer embedded in a consumer product and reflects the actions taken by the components of the microcomputer in a given clock cycle (col. 6, lines 61-67).

Matsunaga. Matsunaga relates to a logic circuit verifying system and method that determines whether two combinational logic circuits are equivalent (col. 1, lines 8-11). The purpose is to verify the functional equivalence of the circuits before and after a circuit configuration is changed (col. 1, lines 13-24). Matsunaga retrieves internal signal lines

assumed to be equivalent from each logic circuit, and then determines whether the logic circuits are equivalent (col. 3, lines 57-61).

The Present Claimed Invention Distinguishes Over the Prior Art

The Linke Reference

The Examiner asserts that the present invention is disclosed in Linke at col. 3, lines 9-16. The cited section of Linke discloses the following: "[S]imulation speed can be increased by grouping a set of elements together and modeling the aggregate behavior of the elements. Then the behavior of the group is simulated as a single object. Such groupings may include only two elements or thousands of elements. Once a grouping is made, the individual behavior of each element is subsumed into the overall behavior of the group."

New independent claim 9 of the present invention recites a method that extracts partial circuits from the circuit to be simulated, determining which partial circuits have equivalent operational characteristics based on their configurations, and compressing the equivalent partial circuits into one circuit, to which circuit simulation is applied. New independent claims 21, 33 and 45 recite similar features. The cited section of Linke discloses that a set of elements is grouped together and simulated as a single group. The cited section does not disclose integrating partial circuits together having equivalent operational characteristics based upon the equivalence of their configurations.

In addition, Linke discloses a technique for carrying out circuit simulation for an electrical system having a first module and a second module. Linke merely describes that circuit simulation is carried out by combining the first module and the second module into one model having a larger scale. In other words, unlike the present invention, Linke does not disclose the configuration in which a plurality of partial circuits that exhibit equivalent operational characteristics are extracted from a LSI circuit and integrated into the circuit model, and then carrying out circuit simulation on the circuit model.

Furthermore, in Linke, electrical interconnections between the first module and the second module are modeled on the presumption that both the first and second modules operate normally, and that the two modules are combined into one model that is suitable for carrying out circuit simulation.

In contrast, in the present invention, a number of module units (i.e., a plurality of partial circuits) each having a scale smaller than a given module (i.e., the circuit to be simulated) are extracted from the given module, and equivalent module units are selected and integrated into one unit before carrying out circuit simulation.

The Matsunaga Reference

The Examiner asserts that "Matsunaga teaches checking for equivalence followed by a merging operation." However, Matsunaga teaches verification of the functional equivalence of two logic circuits by retrieving signal lines assumed to be equivalent from each logic circuit, and then determining whether the logic circuits are equivalent (col. 3, lines 57-61). Matsunaga does not disclose integrating partial circuits together having equivalent operational characteristics based upon the equivalence of their configurations, and determining equivalence of the partial circuits for the purpose of integrating equivalent units to reduce the size of the circuit to be simulated.

In Matsunaga, equivalence of the two logic circuits is verified merely by taking logic functions of these logic circuits into consideration. In other words, unlike the present invention, Matsunaga does not disclose verifying equivalence of a plurality of logic circuits by taking into consideration the configuration of each of the logic circuits.

More specifically, in Matsunaga, even when configurations of the two logic circuits are different, the logic circuits may be regarded as equivalent if the logic functions of the two circuits are the same. However, when two logic circuits have the same logic functions but different circuit configurations, delay time, voltage waveform, and the like are different, as a

matter of course. Therefore, generally, it is not correct to decide that the logic circuits are equivalent, merely on the basis of the logic functions.

A disadvantage of Matsunaga is that the two logic circuits may erroneously be regarded as equivalent, even though the logic circuits have different circuit configurations. Consequently, it becomes impossible to accurately simulate the actual operation of a circuit including these logic circuits, which is an object of circuit simulation.

In contrast, in the present invention, equivalence of two partial circuits is verified on the basis of the configuration of each of the partial circuits. In this case, a plurality of partial circuits having the same delay times and voltage waveforms, as well as the same logic functions, can be integrated into one circuit.

Therefore, according to the present invention, it is possible to shorten the time required for testing a circuit to be simulated by compressing the circuit effectively, and to carry out circuit simulation that is consistent with the actual operation of the circuit.

Further, Matsunaga does not teach, as does claim 9 of the present invention, that a plurality of partial circuits, which are determined to be equivalent, are extracted from a circuit to be simulated. In other words, in Matsunaga, equivalence of a plurality of logic circuits is verified for every circuit element which consists of a plurality of logic circuits and which has a scale much smaller than each of the partial circuits.

Therefore, in Matsunaga, equivalence of a plurality of logic circuits can be verified only in an extremely small area of a circuit to be simulated. Consequently, according to Matsunaga, it is impossible to accurately extract all the partial circuits that are determined to be equivalent. Thus, the circuit cannot be effectively compressed, unlike the present invention.

The remaining independent claims (claim 21, 33 and 45) also recite extracting partial circuits from the circuit to be simulated, determining which partial circuits have equivalent operational characteristics based on their configurations, and compressing the equivalent partial circuits into one circuit, to which circuit simulation is applied. These features are not taught

by the cited references. Therefore, the cited references do not teach all claim limitations of the independent claims of the present invention. Considering dependent claims 9-20, 22-32, and 34-44, for at least the reasons presented above, these dependent claims are deemed to be patentable. Accordingly, Applicant respectfully requests reconsideration and withdrawal of the rejections under § 102.

CONCLUSION

In accordance with the foregoing, it is respectfully submitted that all outstanding rejections have been overcome and/or rendered moot, and further, that all pending claims patentably distinguish over the prior art. Thus, there being no further outstanding rejections, the application is submitted to be in condition for allowance, which action is earnestly solicited.

If there are any formal matters remaining after this response, the Examiner is requested to telephone the undersigned to attend to these matters.

If there are any additional fees associated with filing of this Amendment, please charge the same to our Deposit Account No. 19-3935.

Respectfully submitted,

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